## EE 330 Lecture 4

- Yield
- Statistics Review


## Device and Die Costs

Characterize the high-volume incremental costs of manufacturing integrated circuits
Example: Assume manufacturing cost of an 8 " wafer in a $0.25 \mu$ process is $\$ 800$
Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

$$
\begin{gathered}
n_{\text {trans }} \cong \frac{A_{\text {wafer }}}{A_{\text {trans }}}=\frac{\pi(4 \mathrm{in})^{2}}{(0.25 \mu)^{2}}=5.2 E 11 \\
C_{\text {trans }}=\frac{C_{\text {wafer }}}{n_{\text {trans }}}=\frac{\$ 800}{5.2 E 11}=\$ 15.4 E-9
\end{gathered}
$$

(520 Billion!)
(Trillion, Tera ...10¹2)

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!

## Device and Die Costs

At $\$ 800 / 8$ " wafer, it can be easily shown that:

$$
C_{\text {per unitarea }} \cong \$ 2.5 / \mathrm{cm}^{2}
$$

Example: If the die area of the 741 op amp is $1.8 \mathrm{~mm}^{2}$ (including bonding pads), determine the cost of the silicon needed to fabricate this op amp

$$
C_{741}=\$ 2.5 / \mathrm{cm}^{2} \bullet\left(1.8 \mathrm{~mm}^{2}\right) \cong \$ .05
$$

Actual integrated op amp will be dramatically less if bonding pads are not needed

# Size of Atoms and Molecules in Semiconductor Processes 

| Silicon: | Average Atom Spacing | $2.7{ }^{\circ}$ |
| :---: | :---: | :---: |
|  | Lattice Constant | $5.4 \mathrm{~A}^{\circ}$ |
| $\mathrm{S}_{\mathrm{i}} \mathrm{O}_{2}$ | Average Atom Spacing | $3.5{ }^{\circ}{ }^{\circ}$ |
|  | Breakdown Voltage | 5 to $10 \mathrm{MV} / \mathrm{cm}=5$ to $10 \mathrm{mV} /{ }^{\text {A }}$ |
| Air |  | $20 \mathrm{KV} / \mathrm{cm}$ |

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches

## Defects in a Wafer



- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss


## Yield Issues and Models

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed Hard Faults
- This is the major factor limiting the size of die in integrated circuits
- Wafer scale integration has been a "gleam in the eye" of designers for 3 decades but the defect problem continues to limit the viability of such approaches
- Several different models have been proposed to model the hard faults


## Yield Issues and Models

- Parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)
- The circuits failures associated with these parametric variations are termed Soft Faults
- Increases in area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults


## Hard Fault Model

## $Y_{H}$ <br> 

$Y_{H}$ is the probability that the die does not have a hard fault $A$ is the die area d is the defect density (for some older processes, typically $1 \mathrm{~cm}^{-2}<\mathrm{d}<2 \mathrm{~cm}^{-2}$ ) for some newer processes, typically $0.1 \mathrm{~cm}^{-2}<\mathrm{d}<1 \mathrm{~cm}^{-2}$ )

Industry often closely guards the value of d for their process

Other models, which may be better, have the same general functional form

## Some processes have d under $0.1 \mathrm{~cm}^{-2}$



- Aug 2020 article
- Defect density in per $\mathrm{cm}^{2}$
- Smaller processes even have better defect density!!
- Note continued reduction predicted as process matures


## Example:

Determine the hard yield of a die of area $1 \mathrm{~cm}^{2}$ if the defect density is $1.5 \mathrm{~cm}^{-2}$

$$
\begin{aligned}
& Y_{H}=e^{-A d} \\
& \begin{array}{l}
A=1 \mathrm{~cm}^{2} \\
d=1.5 \mathrm{~cm}^{-2}
\end{array} \\
& Y_{H}=e^{-1 \bullet 1.5}=0.22
\end{aligned}
$$



How good must the defect density be if we must obtain a $95 \%$ yield for the $1 \mathrm{~cm}^{2}$ die?

$$
\left.\begin{array}{rl}
A & =1 \mathrm{~cm}^{2} \\
Y_{H}=0.95
\end{array}\right] \quad \Longrightarrow d=-\ln (0.95) \Longrightarrow d=0.05 \mathrm{~cm}^{-2}
$$

## Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

$$
\sigma=\frac{\rho}{\sqrt{\mathrm{A}_{\mathrm{k}}}}
$$

$\rho$ is a constant dependent upon the architecture and the process
$A_{k}$ is the area of the parameter sensitive area

## Soft Fault Model

$$
P_{\mathrm{SOFT}}=\int_{\mathrm{x}_{\mathrm{MIN}}}^{\mathrm{X}_{\mathrm{MAX}}} \mathrm{f}(\mathrm{x}) \mathrm{dx}
$$

$P_{\text {SOFT }}$ is the soft fault yield
$f(x)$ is the probability density function of the parameter of interest
$X_{\text {MIN }}$ and $X_{\text {MAX }}$ define the acceptable range of the parameter of interest


Some circuits may have several parameters that must meet performance requirements

## Soft Fault Model

If there are k parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

$$
Y_{S}=\prod_{j=1}^{\mathrm{k}} \mathrm{P}_{\mathrm{SOFT}_{\mathrm{j}}}
$$

## Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

$$
\mathrm{Y}=\mathrm{Y}_{\mathrm{H}} \mathrm{Y}_{\mathrm{S}}
$$

## Cost Per Good Die

The manufacturing costs per good die is given by

where $\mathrm{C}_{\text {FabDie }}$ is the manufacturing costs of a fab die and Y is the yield

There are other costs that must ultimately be included such as testing costs, engineering costs, packaging costs, etc.

Example: Assume a die has no soft fault vulnerability, a die area of $1 \mathrm{~cm}^{2}$ and a process has a defect density of $1.5 \mathrm{~cm}^{-2}$
a) Determine the hard yield
b) Determine the manufacturing cost per good die if 8 " wafers are used and if the cost of the wafers is $\$ 1200$

## Solution

a)

$$
\begin{aligned}
& \mathrm{Y}_{\mathrm{H}}=\mathrm{e}^{-\mathrm{Ad}} \\
& \mathrm{Y}=\mathrm{e}^{-1 \mathrm{~cm}^{2} \bullet . .5 \mathrm{~cm}^{2}}=0.22
\end{aligned}
$$

b) $\quad \mathrm{C}_{\text {Good }}=\frac{\mathrm{C}_{\text {FabDie }}}{\mathrm{Y}}$

$$
\begin{gathered}
\mathrm{C}_{\text {FabDie }}=\frac{\mathrm{C}_{\text {Wafer }}}{\mathrm{A}_{\text {Wafer }}} \mathrm{A}_{\text {Die }} \\
\mathrm{C}_{\text {FabDie }}=\frac{\$ 1200}{\pi(4 \mathrm{in})^{2}} 1 \mathrm{~cm}^{2}=\$ 3.82
\end{gathered}
$$

$$
\mathrm{C}_{\text {Good }}=\frac{\$ 3.82}{0.22}=\$ 17.37
$$

## Do you like statistics ?

## Statistics are Real!

## Statistics govern what really happens throughout much of the engineering field!

## Statistics are your Friend !!!!

You might as well know what will happen since statistics characterize what WILL happen in the presence of variability in many processes !

## Statistics Review

Assume x is a random variable of interest
$f(x)=$ Probability Density Function for $x$

$$
\int_{x=-\infty}^{\infty} f(x) d x=1
$$



## Statistics Review

$f(x)=$ Probability Density Function for $x$


## Statistics Review

$$
f(x)=\text { Probability Density Function for } x
$$



## Statistics Review


$\int_{x=-\infty}^{\infty} f(x) d x=1$

$y=\frac{x-\mu}{\sigma}$

$$
\int_{y=-\infty}^{\infty} f_{N}(y) d y=1
$$

Theorem 1: If the random variable $x$ in normally distributed with mean $\mu$ and standard deviation $\sigma$, then $\mathrm{y}=\frac{\mathrm{x}-\mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.
(Normal Distribution and Gaussian Distribution are the same)

## Statistics Review



The random part of many parameters of microelectronic circuits is often assumed to be Normally distributed and experimental observations confirm that this assumption provides close agreement between theoretical and experimental results

The mapping $\quad y=\frac{x-\mu}{\sigma} \quad$ is often used to simplify the statistical characterization of the random parameters in microelectronic circuits $x$ generally is dimensioned, $y$ is dimensionless

## Statistics Review



## Example:

$x$ might be the frequency of oscillation of a ring oscillator used for a clock in a crystal-less digital circuit, x Gaussian (Normal)

Dimensions of $x$ : Hz
Maybe $\mu=550 \mathrm{MHz} \quad \sigma=50 \mathrm{MHz}$
$y=\frac{x-\mu}{\sigma} \quad$ is dimensionless with $\mu_{\mathrm{y}}=0 \quad \sigma_{\mathrm{y}}=1$
$y: \quad N(0,1)$

## Statistics Review



Example:
x might be the offset voltage of an op amp, x Gaussian (Normal)
Dimensions of x : Volts
Typically $\mu=0 \mathrm{~V} \quad \sigma=10 \mathrm{mV}$
$y=\frac{x-\mu}{\sigma} \quad$ is dimensionless with $\mu_{y}=0 \quad \sigma_{y}=1$
$y: \quad N(0,1)$

## Background Information

Theorem 2: If $x$ is a Normal (Gaussian) random variable with mean $\mu$ and standard deviation $\sigma$, then the probability that $x$ is between $x_{1}$ and $x_{2}$ is given by

and where $f_{n}(x)$ is $N(0,1)$


Background Information


Background Information
Observation: The probability that the $N(0,1)$ random variable $x_{n}$ satisfies the relationship $x_{1 n}<x_{n}<x_{2 n}$ is also given by

$$
\mathrm{p}=\mathrm{F}_{\mathrm{n}}\left(\mathrm{x}_{2 \mathrm{n}}\right)-\mathrm{F}_{\mathrm{n}}\left(\mathrm{x}_{1 \mathrm{n}}\right)
$$

where $F_{n}(x)$ is the CDF of $x_{n}$.


Since the $N(0,1)$ distribution is symmetric around $0, p$ can also be expressed as

$$
\mathrm{p}=\mathrm{F}_{\mathrm{n}}\left(\mathrm{x}_{2 \mathrm{n}}\right)-\left(1-\mathrm{F}_{\mathrm{n}}\left(-\mathrm{x}_{1 \mathrm{n}}\right)\right)
$$

Background Information
Observation: In many electronic circuits, a random variable of interest, $x$, is 0 mean Gaussian and the probabilities of interest are characterized by a region defined by the magnitude of the random variable (i.e. $-x_{1}<x<x_{1}$ ).
In these cases, if we define $\mathrm{x}_{N}=\frac{\mathrm{x}-0}{\sigma} \quad$ then $\mathrm{x}_{N}$ is $\mathrm{N}(0,1)$ and
$p\left(-x_{1}<x<x_{1}\right)=\int_{-x_{1}}^{x_{1}} f(x) d x=\int_{-x_{1 n}}^{x_{1 n}} f_{n}(x) d x=F_{n}\left(x_{1 n}\right)-F_{n}\left(-x_{1 n}\right)$
But for the $N(0,1)$ distribution $\quad F_{n}\left(-x_{1 n}\right)=1-F_{n}\left(x_{1 n}\right)$ therefore:

$$
\mathrm{p}=2 \mathrm{~F}_{\mathrm{n}}\left(\mathrm{x}_{1 \mathrm{n}}\right)-1
$$




## Background Information

$$
\mathrm{p}=\mathrm{F}_{\mathrm{n}}\left(\mathrm{x}_{2 \mathrm{n}}\right)-\mathrm{F}_{\mathrm{n}}\left(\mathrm{x}_{1 \mathrm{n}}\right)
$$



$$
\mathrm{p}=2 \mathrm{~F}_{\mathrm{n}}\left(\mathrm{x}_{1 \mathrm{n}}\right)-1
$$



Regardless of whether Gaussian performance requirements are asymmetric or symmetric, the CDF of the $N(0,1)$ distribution (i.e. $\mathrm{F}_{\mathrm{n}}\left(\mathrm{x}_{\mathrm{n}}\right)$ ) can be used to characterize yield

Background Information

## Tables of the CDF of the $N(0,1)$ random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.



## Background Information

Tables of the CDF of the $N(0,1)$ random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

| Far Right |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $Z \quad$ Tail Probabilities |  |  |  |  |  |  |  |  |  |  |
| z | P\{Z to oo \} | I | z | P\{Z to oo \} | 1 | z | P\{Z to oot | I | z | P\{Z to oo \} |
| 2.0 | 0.02275 | I | 3.0 | 0.001350 | I | 4.0 | 0.00003167 | 1 | 5.0 | $2.867 \mathrm{E}-7$ |
| 2.1 | 0.01786 | I | 3.1 | 0.0009676 | I | 4.1 | 0.00002066 | I | 5.5 | $1.899 \mathrm{E}-8$ |
| 2.2 | 0.01390 | I | 3.2 | 0.0006871 | I | 4.2 | 0.00001335 | I | 6.0 | 9.866 E-10 |
| 2.3 | 0.01072 | I | 3.3 | 0.0004834 | I | 4.3 | 0.00000854 | I | 6.5 | 4.016 E-11 |
| 2.4 | 0.00820 | I | 3.4 | 0.0003369 | I | 4.4 | 0.000005413 | I | 7.0 | 1.280 E-12 |
| 2.5 | 0.00621 | I | 3.5 | 0.0002326 | I | 4.5 | 0.000003398 | 1 | 7.5 | 3.191 E-14 |
| 2.6 | 0.004661 | I | 3.6 | 0.0001591 | I | 4.6 | 0.000002112 | I | 8.0 | 6.221 E-16 |
| 2.7 | 0.003467 | I | 3.7 | 0.0001078 | I | 4.7 | 0.000001300 | I | 8.5 | 9.480 E-18 |
| 2.8 | 0.002555 | I | 3.8 | 0.00007235 | I | 4.8 | $7.933 \mathrm{E}-7$ | 1 | 9.0 | $1.129 \mathrm{E}-19$ |
| 2.9 | 0.001866 | I | 3.9 | 0.00004810 | I | 4.9 | $4.792 \mathrm{E}-7$ | I | 9.5 | $1.049 \mathrm{E}-21$ |

## Background Information

Example: Determine the probability that the $N(0,1)$ random variable has magnitude less than 2.6

$$
\mathrm{p}=2 \mathrm{~F}_{\mathrm{n}}(2.6)-1
$$

From the table of the CDF, $F_{n}(2.6)=0.9953$ so $p=.9906$


Background Information
It can be shown that the circuit designer has control of the offset voltage of an op amp and through architecture and sizing of devices can set the standard deviation of the offset voltage at almost any level. Invariably low offset voltages require larger area.
Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5 mV if the offset voltage has a Gaussian distribution with a standard deviation of 2.5 mV and a mean of 0 V .


$$
\begin{array}{r}
p=\int_{-2}^{2} f_{N}(x) d x=F_{N}(2)-F_{N}(-2 \\
p=2 * F_{N}(2)-1
\end{array}
$$

Background Information
Example (continued)

|  |  |
| :---: | :---: | :---: |

http://www.math.unb.ca/~knight/utility/NormTble.htm

## Background Information

## Example (continued)

Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5 mV if the offset voltage has a Gaussian distribution with a standard deviation of 2.5 mV and a mean of OV .


$$
p=2 * F_{N}(2)-1
$$

$\mathrm{F}_{\mathrm{N}}(2)=0.9772$
$p=2 * .9772-1=.9544$

Background Information
Repeat the previous example if the designer decided to reduce the area so that the standard deviation increased to 3.5 mV

Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5 mV if the offset voltage has a Gaussian distribution with a standard deviation of 3.5 mV and a mean of 0 V .


$$
\begin{array}{r}
p=\int_{-1.43}^{1.43} f_{N}(x) d x=F_{N}(1.43)-F_{N}(-1.4 \\
p=2 * F_{N}(1.43)-1
\end{array}
$$

Background Information
Example (continued)

|  |  |
| :--- | :--- | :--- |

http://www.math.unb.ca/~knight/utility/NormTble.htm

Background Information
Repeat the previous example if the designer decided to reduce the area so that the standard deviation increased to 3.5 mV

Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5 mV if the offset voltage has a Gaussian distribution with a standard deviation of 3.5 mV and a mean of 0 V .


This small change in the design dropped the yield from just over $95 \%$ to just under 85\%

Statistical analysis is critical for predicting performance capabilities of many ICs !

## Many Companies Promote the Real Six-Sigma Challenge



From Wikipedia Sept 12021
Six Sigma (6б) is a set of techniques and tools for process improvement. It was introduced by American engineer Bill Smith while working at Motorola in 1986. ${ }^{[11[2]}$ A six sigma process is one in which $99.99966 \%$ of all opportunities to produce some feature of a part are statistically expected to be free of defects.

## Many Companies Promote the Real



From Wikipedia Sept 12021
In 2005 Motorola attributed over $\$ 17$ billion in savings to Six Sigma. ${ }^{[3]}$
By the late 1990s, about two-thirds of the Fortune 500 organizations had begun Six Sigma initiatives with the aim of reducing costs and improving quality. ${ }^{[6]}$

## Yield at the Six-Sigma level

(Assume a Gaussian distribution)


$$
\begin{aligned}
& Y_{6 \text { sigma }}=2 F_{N}(6)-1 \\
& Y_{6 \text { sigma }}=0.9999999980
\end{aligned}
$$

This is approximately 2 defects out of 1 billion parts

## Yield at the Six-Sigma level



This is approximately 2 defects out of 1 billion parts
Would producing ICs with a yield at the six-sigma level be a good goal?
How about smart phones with defects at this level? (approx. 1.4B sold in 2020)

How about automobiles? (approx. 78 million produced in 2020)

## Six-Sigma or Else !!

How serious is the "or Else" in the six-sigma programs?



## Six-Sigma or Else !!

It is assumed that the performance or yield will drop, for some reason, by 1.5 sigma after a process has been established

Initial "six-sigma" solutions really expect only 4.5 sigma performance in steady-state production

Assumption: Processes of interest are Gaussian (Normal)
4.5 sigma performance corresponds to 3.4 defects in a million

Observation: Any Normally distributed random variable can be mapped to a $\mathrm{N}(0,1)$ random variable by subtracting the mean and dividing by the variance

## Meeting the Real Six-Sigma Challenge



## Six-Sigma or Else !!

Highly Statistical Concept !

## The Six-Sigma Challenge

Two-sided capability:


Long-term Capability
Tails are 6.8 parts in a million
Short-term Capability
Tail is 2 parts in a billion

Example: Determine the maximum die area if the circuit yield is to initially meet the "six sigma" challenge for hard yield defects (Assume a defect density of $1 \mathrm{~cm}^{-2}$ and only hard yield loss). Is it realistic to set six-sigma die yield expectations on the design and process engineers?

## Solution:

The "six-sigma" challenge requires meeting a 6 standard deviation yield with a Normal $(0,1)$ distribution


$$
\begin{aligned}
& Y_{6 \text { sigma }}=2 \mathrm{~F}_{\mathrm{N}}(6)-1 \\
& \text { Recall: } \quad F_{N}(6)=0.9999999980 \\
& Y_{6 \text { sigma }}=0.999999996
\end{aligned}
$$

Solution cont:

$$
\begin{gathered}
Y_{H}=e^{-A d} \quad A=\frac{-\ln \left(Y_{H}\right)}{d} \\
A=\frac{-\ln (.9999999980)}{1 \mathrm{~cm}^{-2}}=4.0 \mathrm{E}-9 \mathrm{~cm}^{2}=40 \mathrm{E} 6(\mathrm{~A})^{2}
\end{gathered}
$$



Consider a 20 nm process with 10x area overhead

$$
\begin{gathered}
\mathrm{A}_{\text {TRAN }}=10^{*}(200)^{2}(\AA)^{2}=4 \mathrm{E}\left(\AA(\AA)^{2}\right. \\
\mathrm{n}=\frac{40 \mathrm{E}(\stackrel{\circ}{\mathrm{~A}})^{2}}{4 \mathrm{E} 5\left({ }^{\circ} \mathrm{A}\right)^{2}}=100
\end{gathered}
$$

This is comparable to the area required to fabricate about 100 minimumsized transistors in a state of the art 20nm process

Solution cont:
Is it realistic to set six-sigma die hard yield expectations on the design and process engineers?

The best technologies in the world have orders of magnitude too many defects to build any useful integrated circuits with die yields that meet six-sigma performance requirements !!

Arbitrarily setting six-sigma design requirements will guarantee financial disaster !!

## Meeting the Real Six-Sigma Challenge



## Six-Sigma or Else !!

## Meeting the Real Six-Sigma Challenge



Improving a yield by even one sigma often is VERY challenging !!

## Meeting the Real Six-Sigma Challenge



So, how has Motorola prospered with "meeting" the 6sigma challenge?

MOTOROLA


## Stay Safe and Stay Healthy !

## End of Lecture 4

